IEEE *Xplore®*
RELEASE 2.1

Welcome United States Patent and Trademark Office

View Selected Items   BROWSE   SEARCH   IEEE XPLORE GUIDE

Results for " ((luculli)<in>metadata) "   ✉ e-mail
Your search matched 9 of 1415139 documents. You selected 6 items.

Display Format: ○ Citation   ◉ Citation & Abstract

» Download Citations

Article Information   View: 1-6 |

Citation & Abstract ▼

ASCII Text   ▼ »

» Learn more

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

1. A cache-aware scheduling algorithm for embedded systems
    Luculli, G.; Di Natale, M.
    Real-Time Systems Symposium, 1997. Proceedings., The 18th IEEE
    2-5 Dec 1997
    Page(s): 199-209
    Digital Object Identifier 10.1109/REAL.1997.641282
    Summary: The paper presents a methodology for scheduling real time tasks in embedded systems where th
    at design time and does not change at execution time (static systems) and where the cache miss costs are s
    compared to t.....

    AbstractPlus | Full Text: PDF   IEEE CNF

2. A software tool for the timing analysis of embedded software
    Luculli, G.; Sangiovanni-Vincentelli, A.
    Electrotechnical Conference, 2000. MELECON 2000. 10th Mediterranean
    Volume: 2 2000
    Page(s): 754- 757 vol.2
    Digital Object Identifier 10.1109/MELCON.2000.880043
    Summary: The presence of real-time software modules which interact with specific hardware architectures i
    embedded applications. New methods and tools are needed for program analysis and the validation of these
    analysi.....

    AbstractPlus | Full Text: PDF   IEEE CNF

3. Analysis of DSP-kernel software by implicit cache simulation
    Luculli, G.; Sangiovanni-Vincentelli, A.
    Engineering of Computer Based Systems, 2001. ECBS 2001. Proceedings. Eighth Annual IEEE Internationa
    Workshop on the
    2001
    Page(s): 282-288
    Digital Object Identifier 10.1109/ECBS.2001.922434
    Summary: We introduce a new approach to performance analysis of DSP-kernel software, based on high-le
    called implicit cache simulation. The method can take into account any kind of instruction cache as well as c
    We show.....

    AbstractPlus | Full Text: PDF   IEEE CNF

4. An ISA-retargetable framework for embedded software analysis
    Luculli, G.
    Engineering of Computer-Based Systems, 2003. Proceedings. 10th IEEE International Conference and Worl
    7-10 April 2003
    Page(s): 183- 190
    Digital Object Identifier 10.1109/ECBS.2003.1194798
    Summary: Industry requires new advanced tools and methodologies for the design of complex system-on-c
    STMicroelectronics we developed an innovative retargetable technology for the analysis and optimization of
    In this paper.....

    AbstractPlus | Full Text: PDF   IEEE CNF

5.
    Retargetable tools for embedded software

Luculli, G.
<u>EUROCON 2003. Computer as a Tool. The IEEE Region 8</u>
Volume: 1 22-24 Sept. 2003
Page(s): 52- 56 vol.1
Summary: Today, the advent of the multi-million transistor chip offers the opportunity to provide more integ
into a single silicon die. This is both a clear advantage to improve existing products and a hard challenge to

<u>AbstractPlus</u> | Full Text: <u>PDF</u>   IEEE CNF

6.   **Efficient and effective simulation of memory maps for system-on-chip**
Luculli, G.
<u>Engineering of Computer-Based Systems, 2004. Proceedings. 11th IEEE International Conference and Worl</u>
 24-27 May 2004
Page(s): 242- 247
Digital Object Identifier 10.1109/ECBS.2004.1316705
Summary: The design of complex system-on-chip (SOC) requires new methods and tools for the optimizati
software which is executed on ever more complex hardware architectures. The tuning of the memory subsys
difficult due to th.....

<u>AbstractPlus</u> | Full Text: <u>PDF</u>   IEEE CNF
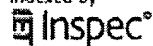

View: **1-6** | <u>**View Search**</u>

Help   Contact Us   Privac

Indexed by
Inspec°

Google

Web   Images   Video^{New!}   News   Maps   **more »**

| specification for machine instruction with class | Search | Advanced Search Preferences |

Web Results **11 - 20** of about **3,900,000** for <u>specification</u> for <u>machine</u> <u>instruction</u> with <u>class</u> <u>definition</u>. (0.1·

Tip: Click to get a definition of: <u>specification</u> <u>machine</u> <u>instruction</u> <u>class</u>
      Or just click on the underlined words in the above colored bar

DDML <u>Specification</u>, Version 1.0
Document **Definition** Markup Language (DDML) **Specification**, Version 1.0 ... Note that
including a DDML processing **instruction** in letter.ddm that points to ...
www.w3.org/TR/NOTE-ddml - 122k - <u>Cached</u> - <u>Similar pages</u>

[PDF] <u>CMDL: a **class**-based **machine** description language for co-generation ...</u>
File Format: PDF/Adobe Acrobat - <u>View as HTML</u>
oriented language, if the **definition** of **class** A includes. another **class** B, the member ...
scriptions of various aspects of a **machine** (**instruction** syn- ...
www.cs.umass.edu/~moss/papers/ipdps-2004-cmdl.pdf - <u>Similar pages</u>

Security and the <u>class</u> verifier
If, for example, a Java virtual **machine** discovers during early loading that it can't find a
certain referenced **class**, it doesn't throw a "**class definition** ...
www.javaworld.com/javaworld/jw-10-1997/jw-10-hood.html - <u>Similar pages</u>

Turing **Machine**
Instructions for a Turing **machine** consist in specified conditions under which ... Each 4-
tuple in the **machine specification** will be encoded as a sequence of ...
plato.stanford.edu/entries/turing-**machine**/ - <u>Similar pages</u>

programming language: **Definition** and Much More From Answers.com
Once we build concepts around a **class definition**, we have a separate package ... Some
compilers translate a program into **machine** code (**instructions** that can ...
www.answers.com/topic/programming-language - 157k - <u>Cached</u> - <u>Similar pages</u>

SGI - Products: Software: IRIX: Tools: ProDev Workshop
It permits automatic or manual **specification** of process groups and provides ... Similarly,
when viewing a **class definition**, users can choose to view just ...
www.sgi.com/products/software/irix/tools/prodev.html - 25k - <u>Cached</u> - <u>Similar pages</u>

[PDF] <u>ILLINOIS DEPARTMENT OF CENTRAL MANAGEMENT SERVICES **CLASS** ...</u>
File Format: PDF/Adobe Acrobat - <u>View as HTML</u>
CLASS SPECIFICATION. REPRODUCTION SERVICE TECHNICIAN SERIES. **CLASS**
TITLE ... equipment; receives **instruction** regarding methods used to calculate such
items ...
www.state.il.us/cms/persnl/specs/38204.pdf - <u>Similar pages</u>

Glossary
See Java **Specification** Request. JVM. See Java virtual **machine**. large object (LOB). The
class of SQL data type that is further divided into Internal LOBs and ...
www.stanford.edu/dept/itss/docs/oracle/10g/appdev.101/b10794/glossary.htm - 86k -
<u>Cached</u> - <u>Similar pages</u>

<u>Class Definition for Class 712 - ELECTRICAL COMPUTERS AND DIGITAL ...</u>
This subclass is indented under the **class definition**. ... This subclass is directed to

**instruction** processing and **machine** level **Instruction** execution. ...
www.uspto.gov/go/**class**ification/uspc712/defs712.htm - 310k - <u>Cached</u> - <u>Similar pages</u>

<u>SPEC: KEY DATA OPERATIONS CALIFORNIA STATE PERSONNEL BOARD ...</u>
Schem **Class** Code Code **Class** CJ50 1419 Key Data Operator CJ40 1420 Key Data ...
DEFINITION OF LEVELS KEY DATA OPERATOR This is the entry, training and ...
www.dpa.ca.gov/textdocs/specs/s1/s1419.txt - 11k - <u>Cached</u> - <u>Similar pages</u>

| specification for machine instruction | **Search** |
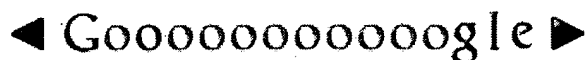
<u>Search within results</u> | <u>Language Tools</u> | <u>Search Tips</u>

<u>Google Home</u> - <u>Advertising Programs</u> - <u>Business Solutions</u> - <u>About Google</u>

©2006 Google

PﬔRTAL
USPTO

Search: ⊙ The ACM Digital Library   ○ The Guide

SLED

SEARCH

THE ACM DIGITAL LIBRARY

▪ Feedback Report a problem Satisfaction survey

Term used **SLED**

Found **78** of **185,942**

Sort results by | relevance ▼ |

💾 Save results to a Binder

Try an Advanced Search
Try this search in The ACM Guide

Display results | expanded form ▼ |

❓ Search Tips

☐ Open results in a new window

Results 1 - 20 of 78

Result page: **1** 2 3 4 next

Relevance scale ☐ ▭ ▬ ■ ■

1 Designing computer systems with MEMS-based storage ■

Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger
November 2000 **ACM SIGOPS Operating Systems Review , ACM SIGARCH Computer Architecture News , Proceedings of the ninth international conference on Architectural support for programming languages and operating systems ASPLOS-IX**, Volume 34 , 28 Issue 5 , 5
Publisher: ACM Press

Full text available: 📄 pdf(439.06 KB)   Additional Information: full citation, abstract, references, citings, index terms

> For decades the RAM-to-disk memory hierarchy gap has plagued computer architects. An exciting new storage technology based on microelectromechanical systems (MEMS) is poised to fill a large portion of this performance gap, significantly reduce system power consumption, and enable many new applications. This paper explores the system-level implications of integrating MEMS-based storage into the memory hierarchy. Results show that standalone MEMS-based storage reduces I/O stall times by 4-74X over ...

2 Designing computer systems with MEMS-based storage ■

Steven W. Schlosser, John Linwood Griffin, David F. Nagle, Gregory R. Ganger
November 2000 **ACM SIGPLAN Notices**, Volume 35 Issue 11
Publisher: ACM Press

Full text available: 📄 pdf(439.06 KB)   Additional Information: full citation, abstract, references, index terms

> For decades the RAM-to-disk memory hierarchy gap has plagued computer architects. An exciting new storage technology based on microelectromechanical systems (MEMS) is poised to fill a large portion of this performance gap, significantly reduce system power consumption, and enable many new applications. This paper explores the system-level implications of integrating MEMS-based storage into the memory hierarchy. Results show that standalone MEMS-based storage reduces I/O stall times by 4--74X ove ...

3 Modeling and performance of MEMS-based storage devices ■

John Linwood Griffin, Steven W. Schlosser, Gregory R. Ganger, David F. Nagle
June 2000 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2000 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '00**, Volume 28 Issue 1
Publisher: ACM Press

Full text available: 📄 pdf(892.07 KB)   Additional Information: full citation, abstract, references, citings, index terms

MEMS-based storage devices are seen by many as promising alternatives to disk drives. Fabricated using conventional CMOS processes, MEMS-based storage consists of thousands of small, mechanical probe tips that access gigabytes of high-density, nonvolatile magnetic storage. This paper takes a first step towards understanding the performance characteristics of these devices by mapping them onto a disk-like metaphor. Using simulation models based on the mechanics equations governing the device ...

4 Specifying representations of machine instructions

Norman Ramsey, Mary F. Fernández
May 1997 **ACM Transactions on Programming Languages and Systems (TOPLAS),**
        Volume 19 Issue 3
Publisher: ACM Press

Full text available: pdf(320.62 KB)   Additional Information: full citation, abstract, references, citings, index terms

We present SLED, a specification language for Encoding and Decoding, which describes, abstract, binary, and assembly-language representations of machine instructions. Guided by a SLED specification, the New Jersey Machine-Code Toolkit generates bit-manipulating code for use in applications that process machine code. Programmers can write such applications at an assembly language level of abstraction, and the toolkit enables the applications to recognize and emit the binary representations u ...

Keywords: compiler generation, decoding, encoding, machine code, machine description, object code, relocation

5 Using MEMS-based storage in computer systems---device modeling and management

Bo Hong, Scott A. Brandt, Darrell D. E. Long, Ethan L. Miller, Ying Lin
May 2006 **ACM Transactions on Storage (TOS),** Volume 2 Issue 2

Publisher: ACM Press

Full text available: pdf(649.15 KB)   Additional Information: full citation, abstract, references, index terms

MEMS-based storage is an emerging nonvolatile secondary storage technology. It promises high performance, high storage density, and low power consumption. With fundamentally different architectural designs from magnetic disk, MEMS-based storage exhibits unique two-dimensional positioning behaviors and efficient power state transitions. We model these low-level, device-specific properties of MEMS-based storage and present request scheduling algorithms and power management strategies that exploit ...

Keywords: MEMS-based storage, power management, request scheduling

6 MEMS-based integrated-circuit mass-storage systems

L. Richard Carley, Gregory R. Ganger, David F. Nagle
November 2000 **Communications of the ACM,** Volume 43 Issue 11

Publisher: ACM Press

Full text available: pdf(577.78 KB)
                   html(41.51 KB)   Additional Information: full citation, references, citings, index terms

7 Automatic checking of instruction specifications

Mary Fernández, Norman Ramsey
May 1997 **Proceedings of the 19th international conference on Software engineering**

Publisher: ACM Press
Full text available: pdf(2.07 MB)   Additional Information: <u>full citation</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Keywords: application generators, machine-code toolkit, specification testing

8 <u>A case for redundant arrays of inexpensive disks (RAID)</u>
David A. Patterson, Garth Gibson, Randy H. Katz
June 1988 **ACM SIGMOD Record , Proceedings of the 1988 ACM SIGMOD international conference on Management of data SIGMOD '88**, Volume 17 Issue 3
Publisher: ACM Press

Full text available: pdf(1.20 MB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>citings</u>, <u>index terms</u>

Increasing performance of CPUs and memories will be squandered if not matched by a similar performance increase in I/O. While the capacity of Single Large Expensive Disks (SLED) has grown rapidly, the performance improvement of SLED has been modest. Redundant Arrays of Inexpensive Disks (RAID), based on the magnetic disk technology developed for personal computers, offers an attractive alternative to SLED, promising improvements of an order of magnitude in performance, reliability, ...

9 <u>Real-world applications: papers: On evolving buffer overflow attacks using genetic programming</u>
Hilmi Güneş Kayacik, Malcolm Heywood, Nur Zincir-Heywood
July 2006 **Proceedings of the 8th annual conference on Genetic and evolutionary computation GECCO '06**
Publisher: ACM Press
Full text available: pdf(301.22 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

In this work, we employed genetic programming to evolve a "white hat" attacker; that is to say, we evolve variants of an attack with the objective of providing better detectors. Assuming a generic buffer overflow exploit, we evolve variants of the generic attack, with the objective of evading detection by signature-based methods. To do so, we pay particular attention to the formulation of an appropriate fitness function and partnering instruction set. Moreover, by making use of the intron behavi ...

Keywords: intrusion detection systems, linear genetic programming, mimicry attacks

10 <u>High-level views on low-level representations</u>
Iavor S. Diatchki, Mark P. Jones, Rebekah Leslie
September 2005 **ACM SIGPLAN Notices , Proceedings of the tenth ACM SIGPLAN international conference on Functional programming ICFP '05**, Volume 40 Issue 9
Publisher: ACM Press
Full text available: pdf(176.18 KB)   Additional Information: <u>full citation</u>, <u>abstract</u>, <u>references</u>, <u>index terms</u>

This paper explains how the high-level treatment of datatypes in functional languages—using features like constructor functions and pattern matching—can be made to coexist with *bitdata*. We use this term to describe the bit- level representations of data that are required in the construction of many different applications, including operating systems, device drivers, and assemblers. We explain our approach as a combination of two language extensions, each of which could potenti ...

Keywords: bit manipulation, bitdata, bitfields, data representation, pattern matching, polymorphism, qualified types, views

11 The role of lexico-semantic feedback in open-domain textual question-answering

Sanda Harabagiu, Dan Moldovan, Marius Paşca, Rada Mihalcea, Mihai Surdeanu, R☐zvan Bunescu, Roxana Gîrju, Vasile Rus, Paul Mor☐rescu

July 2001 **Proceedings of the 39th Annual Meeting on Association for Computational Linguistics ACL '01**

Publisher: Association for Computational Linguistics

Full text available: pdf(112.79 KB)   Additional Information: full citation, abstract, references

This paper presents an open-domain textual Question-Answering system that uses several feedback loops to enhance its performance. These feedback loops combine in a new way statistical results with syntactic, semantic or pragmatic information derived from texts and lexical databases. The paper presents the contribution of each feedback loop to the overall performance of 76% human-assessed precise answers.

12 Posters: Acquisition and maintenance of constraints in engineering design

Suraj Ajit, Derek Sleeman, David W. Fowler, David Knott, Kit Hui

October 2005 **Proceedings of the 3rd international conference on Knowledge capture K-CAP '05**

Publisher: ACM Press

Full text available: pdf(95.33 KB)   Additional Information: full citation, abstract, references, index terms

The Designers' Workbench is a system, developed by the Advanced Knowledge Technologies (AKT) consortium to support designers in large organizations, such as Rolls-Royce, by making sure that a design is consistent with the specification for the particular design as well as with the company's design rule book(s). Currently, to capture the constraint information, a domain expert (design engineer) has to work with a knowledge engineer to identify the constraints, and it is then the task of the know ...

Keywords: ConEditor, application conditions, constraints, maintenance

13 Machine-adaptable dynamic binary translation

David Ung, Cristina Cifuentes

January 2000 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN workshop on Dynamic and adaptive compilation and optimization DYNAMO '00**, Volume 35 Issue 7

Publisher: ACM Press

Full text available: pdf(1.23 MB)   Additional Information: full citation, abstract, references, citings, index terms

Dynamic binary translation is the process of translating and optimizing executable code for one machine to another at runtime, while the program is "executing" on the target machine.

Dynamic translation techniques have normally been limited to two particular machines; a competitor's machine and the hardware manufacturer's machine. This research provides for a more general framework for dynamic translations, by providing a framework based on specifications of machines that ...

Keywords: binary translation, dynamic compilation, dynamic execution, emulation, interpretation

14 Using MEMS-based storage in computer systems---MEMS storage architectures

Bo Hong, Feng Wang, Scott A. Brandt, Darrell D. E. Long, Thomas J. E. Schwarz

February 2006 **ACM Transactions on Storage (TOS)**, Volume 2 Issue 1
Publisher: ACM Press
Full text available: pdf(472.59 KB)   Additional Information: full citation, abstract, references, index terms

As an emerging nonvolatile secondary storage technology, MEMS-based storage exhibits several desirable properties including high performance, high storage volumic density, low power consumption, low entry cost, and small form factor. However, MEMS-based storage provides a limited amount of storage per device and is likely to be more expensive than magnetic disk. Systems designers will therefore need to make trade-offs to achieve well-balanced designs. We present an architecture in which MEMS dev ...

Keywords: MEMS-based storage, cost-performance, economic lifetime, hybrid storage devices, maintenance strategies, storage enclosures

15 Interposed proportional sharing for a storage service utility

Wei Jin, Jeffrey S. Chase, Jasleen Kaur
June 2004 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the joint international conference on Measurement and modeling of computer systems SIGMETRICS '04/Performance '04**, Volume 32 Issue 1
Publisher: ACM Press

Full text available: pdf(339.02 KB)   Additional Information: full citation, abstract, references, citings, index terms

This paper develops and evaluates new share-based scheduling algorithms for differentiated service quality in network services, such as network storage servers. This form of resource control makes it possible to share a server among multiple request flows with probabilistic assurance that each flow receives a specified minimum share of a server's capacity to serve requests. This assurance is important for safe outsourcing of services to shared utilities such as Storage Service Providers.Our appr ...

Keywords: differentiated service, fair sharing, multiprocessor scheduling, performance isolation, proportional sharing, quality of service, storage services, utility computing, weighted fair queuing

16 Interface to architecture: integrating technology into the environment in the Brain Opera

Maggie Orth
August 1997 **Proceedings of the conference on Designing interactive systems: processes, practices, methods, and techniques**
Publisher: ACM Press
Full text available: pdf(1.41 MB)   Additional Information: full citation, references, index terms

Keywords: architecture, collaboration, design, environment, furniture, interface, opera, physical interface, sensor, theater

17 TDL: a hardware description language for retargetable postpass optimizations and analyses

Daniel Kästner
September 2003 **Proceedings of the second international conference on Generative programming and component engineering GPCE '03**
Publisher: Springer-Verlag New York, Inc.

Additional Information: full citation, abstract, references, citings, index

Full text available: 📄 pdf(433.80 KB)   terms

The hardware description language TDL has been designed with the goal to generate machine-dependent postpass optimizers and analyzers from a concise specification of the target processor. TDL is assembly-oriented and provides a generic modeling of irregular hard-ware constraints that are typical for many embedded processors. The generic modeling supports graph-based and search-based optimization algorithms. An important design goal of TDL was to achieve extendibility, so that TDL can be easily i ...

18 Technical correspondence: Retargetable cross compilation techniques: comparison and analysis of GCC and Zephyr

Dai Guilan, Tian Jinlan, Zhang Suqin, Jiang Weidu, Dai Jun
June 2002 **ACM SIGPLAN Notices**, Volume 37 Issue 6

Publisher: ACM Press

Full text available: 📄 pdf(571.95 KB)   Additional Information: full citation, abstract, references

Both GCC and Zephyr are representative complier infrastructures. The paper explores the basic questions that need to be resolved to develop compilers for the support of multiple source languages and targets analyses and compares their architectures and key retargetable cross compilation techniques, summarizes the merits and shortcomings, respectively, and draws a conclusion that the Zephyr infrastructure has the advantage over GCC to an extent.

Keywords: GCC, compiler infrastructures, cross compilation, intermediate representations, machine descriptions, zephyr

19 Optimising hot paths in a dynamic binary translator

David Ung, Cristina Cifuentes
March 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 1

Publisher: ACM Press

Full text available: 📄 pdf(890.10 KB)   Additional Information: full citation, abstract, citings, index terms

In dynamic binary translation, code is translated "on the fly" at run-time, while the user perceives ordinary execution of the program on the target machine. Code fragments that are frequently executed follow the same sequence of flow control over a period of time. These fragments form a hot path and are optimised to improve the overall performance of the program.Multiple hot paths may also exist in programs. A program may choose to execute in one hot path for some time, but later switch to anot ...

Keywords: binary translation, dynamic compilation, dynamic execution, run-time profiling

20 Optimization of custom MOS circuits by transistor sizing

Andrew R. Conn, Paula K. Coulman, Ruud A. Haring, Gregory L. Morrill, Chandu Visweswariah
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: 📄 pdf(68.85 KB)   Additional Information: full citation, abstract, references, citings, index
📄 Publisher Site   terms

Optimization of a circuit by transistor sizing is often a slow, tedious and iterative manual process which relies on designer intuition. Circuit simulation is carried out in the inner loop of this tuning procedure. Automating the transistor sizing process is an important step towards being able to rapidly design high-performance, custom circuits. JiffyTune is a new circuit optimization tool that automates the tuning task. Delay, rise/fall time, area and

power targets are accommodated. Each (weig ...

Keywords: Circuits, transistor sizing, optimization, simulation, gradients.

Results 1 - 20 of 78   Result page: **1**   2   3   4   next

Useful downloads: Adobe Acrobat   QuickTime   Windows Media Player   Real Player